IN THE SPECIFICATION:

Please amend the specification as follows:

Paragraph 60: please replace this paragraph with the following rewritten paragraph:

FIG. 8 shows a system block diagram of a scheduler, according to another embodiment of the present invention. As shown in FIG. 8, scheduler 440 includes request generator 441, first-stage arbiters 442, second-stage arbiters 443, decision generators 444 and 445, and matching combiner 446. Note that FIG. 8 shows the first-stage arbiters and second-stage arbiters at a first time, t_1, and at a second time, t_2. At the first time, t_1, the first-stage arbiters and second-stage arbiters are labeled as ~~422~~ 442 and 443, respectively; at the second time, t_2, the first-stage arbiters and second-stage arbiters are labeled as ~~422'~~ 442' and 443', respectively. First-stage arbiters 442 and 442' are physically the same devices; second-stage arbiters 443 and 443' are physically the same devices. FIG. 8 shows the transmission of arbitration signals from first-stage arbiters 442 and second-stage arbiters 443 (determined during the first time, t_1) to second-stage arbiters 443' and first-stage arbiters 442', respectively (determined during the second time t_2).